IJAREEIE

e-ISSN: 2278-8875
p-ISSN: 2320-3765

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

Volume 11, Issue 3, March 2022

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

Impact Factor: 7.282

| e-ISSN: 2278 – 8875, p-ISSN: 2320 – 3765| www.ijareeie.com | Impact Factor: 7.282|

|| Volume 11, Issue 3, March 2022 ||

DOI:10.15662/IJAREEIE.2022.1103025

An Efficient Least Cell Design of QCA Adder-Subtractor Circuit

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ABSTRACT: Nowadays Quantum-dot cellular automata technology seems to be very attractive in the research field. It can perform any arithmetic and logical operations. In this paper, we design a QCA circuit. The aim of this paper is to propose a least cell count design of adder-subtractor circuit. The proposed QCA adder-subtractor circuit is designed based on the new concept. It requires only two majority gates for designing. The output is shown with the QCA Designer tool and then the result is compared with the result of previous papers presenting adder - subtractor together.

KEYWORDS: Quantum-dot cellular automata, adder- subtractor, majority gate, less cell count.

I.INTRODUCTION

Form very long time CMOS technology gives very good real-time applications in integrated circuit field. But now we found CMOS technology also have some flaws. One of the flaw of CMOS technology is that when we are trying to gain speed it starts consuming more power and if we are trying to reduce power as energy consumption is also one of the very important factors while designing any circuit, so its speed decreases automatically. Another flaw of CMOS technology is decreasing transistor size comes to its limits, if we are trying to reduce transistor current size then due to leakage current problems our device can't able to switch off properly and because of it, more heat dissipation is seen in the chip. So because of these flaws designer was continuously looking for new technology that provides greater integration in low power consumption. Now they found a new technology that becomes a good solution for this problem. This new technology able to design digital circuits which have very high speed and also consume ultra-low power. The name of this technology is Quantum-dot cellular automata which can be abbreviated as QCA. Researches on it shows that it can able to achieve unexpectedly high device density which can be up to 1012 devices/cm2 .There is no role of voltage and current in QCA. Its work is based on the coulombic interaction principle between electrons inside quantum dots. Adder plays a very important role in designing all other operations in digital circuits. We can design adder and subtractor separately. There are many research papers continuously working on the best design of adder as well as subtractor circuits. Currently, the best design of QCA adder with the least cell is 19 cells and subtractor as 20 cells. In total if we want to make a circuit that can perform both adding and subtracting operations so from merging these separate best designs, we required 19 cells summing with 20 cells so we get 39 cells. So this paper aims to present an adder-subtractor circuit that can able to perform both adding as well as subtracting operations, design should possibly have the least number of cells that can decrease area. Here we use the majority gate to design our adder-subtractor circuit.

The adder-subtractor was developed in 2020 using QCA technology by Sir R. Marshal & Sir G. Lakshminarayanan with 38 cells[8]. This paper applies a new concept for design an adder-subtractor circuit. This design shows a significant reduction in all important parameters of design.

The organization of this paper is quite simple which are as follows: Firstly we discuss the basics of QCA technology in section 2. Then, our proposed design with its simulation is present in section 3. Section 4 discusses the result of obtained simulation and there is also a comparison that compared all important parameters like area, cell count of the proposed design in this paper with the previous design. At last section 5 concluded a simple conclusion. Last section presents references to use for making this paper.

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II.BACKGROUND OF QCA TECHNOLOGY

Symmetric square cells are used to describe the QCA devices. With the help of these square cells we can not only make any logic gates but also with it we can make any memory circuit. The different patterns can make putting these cells either side by side or to a different degree. Each of such specific patterns shows the required logic function. QCA has two electrons moving inside four quantum dots present in the cell. These two electrons are present diagonally in cells. There are two ways in which electrons present diagonally inside the cell. One way give the output '0' while another one gives logic '1'[10], as diagram it can be depicted in the figure below as follows:

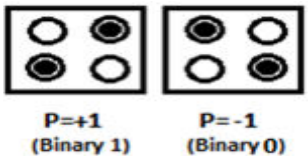

Fig 1: Quantum cellular automata cells with polarizations
P= +1 for Binary 1 and P= -1 for Binary 0.

For design purposes, we have to know the basic knowledge of QCA wires. The only purpose of wire in the real world is to transfer data from one point to another.QCA wires full fill the same purpose. It is the simplest design in which if we place cells side by side in a row, then it can propagate signal from its starting point to ending point. There are two types of QCA wire connection with its difference in degree reflect the change in output[2], seen in the figure below as follows:

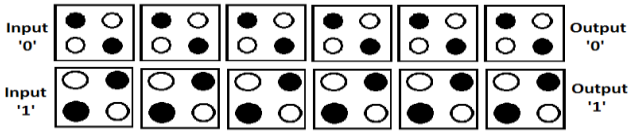

Fig 2: QCA wire(90 degrees)

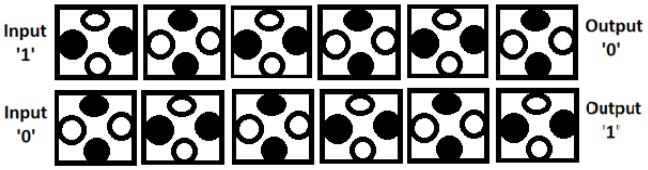

Fig 3: QCA wire (45 degrees)

In QCA technology all the basic gates can be designed using two gates which are the majority gate and inverter. The inverter can invert the input signal. Simply if two cells are arranged diagonally it starts behaving as an inverter and shows the inverted signal as output. The inverter is shown in the figure below as follows:

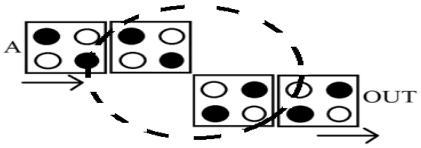

Fig 4: Inverter as cells placed at 45 degrees from one another

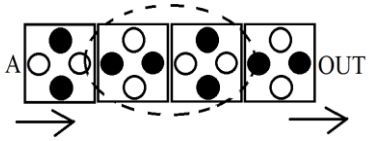

Fig 5: Inverter design placed side by side in a row

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The core of the design present in this paper is a majority gate. The majority voter gate is designed to form a cross structure with five cells, in which the cell present in the centre is called a device cell. We can give three inputs to it and the other fourth cell gives the output. The figure for the majority gate is shown below[10]:

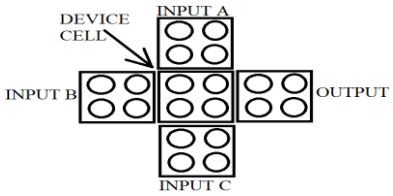

Fig 6: Block diagram of majority voter gate

The logical function representation of majority voter gate is shown below as follows:
F(A,B,C)= AB+AC+BC
Here we simply have three inputs as A,B and C and one output.

When we fix polarization of any one of the input of Majority gate to either "0" or "1", it can be used successively as AND or OR gate .

Let us fix input C to 1 then we get output as A+B whereas fixing input C to 0 the output we get output as A.B. The logic function representation for majority voter gate as AND and OR gate is shown below as follows:
M(A,B,1)=A+B
M(A,B,0)=A.B

A	B	C	OUT	
0	0	0	0	AND Logic When one input is set to "0"
0	0	1	0	
0	1	0	0	
0	1	1	1	
1	0	0	0	OR Logic When one input is set to "1"
1	0	1	1	
1	1	0	1	
1	1	1	1	

Table 1: Truth table of majority voter gate.

The three input XOR gate is simply passes '1' if it get odd number of '1' at input side and because of this it is called as a odd detector.The present most efficient least cell QCA XOR gate design is made by adding three more cells in majority voter gate design and is presented in below as follows[11]:

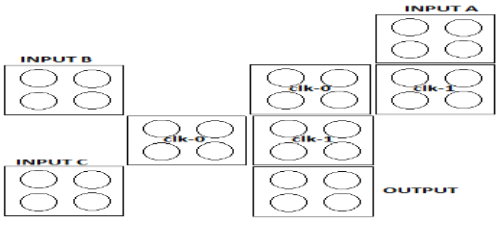

Fig 7:XOR gate in QCA

The logic function representation of XOR is shown below as follows:
F(A,B,C)= A⊕B⊕C=ABC+A'B'C+AB'C'+A'BC'
Here we simply have three inputs as A,B and C and one output.

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The truth table satisfying the above mentioned logical function of XOR gate is shown below:

Input			Output
A	B	C	F=A⊕B⊕C
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table 2: Truth table of XOR gate.

III.PROPOSED DESIGN WITH ITS SIMULATION RESULT

This section presents the basic information about the adder-subtractor circuit and then presents the proposed design.QCA Designer simulation tool can be used to stimulate computational digital circuits constructed using QCA. It can be very simple to construct complex Quantum Dot cellular Circuits using this very simple tool.

An adder-subtractor circuit can perform both addition as well as subtraction operation in a single circuit. It works on three 1-bit numbers taken as input A, input B, and input C, and the one output shows the sum/diff bit and one of the other two output shows the carry bit and the other one shows borrow bit. The below figure present the block diagram for adder- subtractor circuit with its truth table:

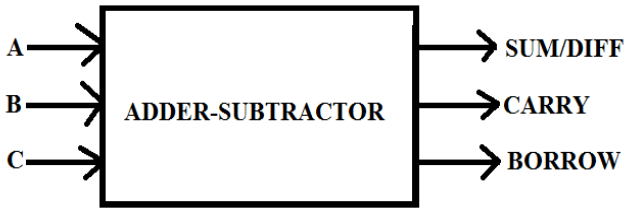
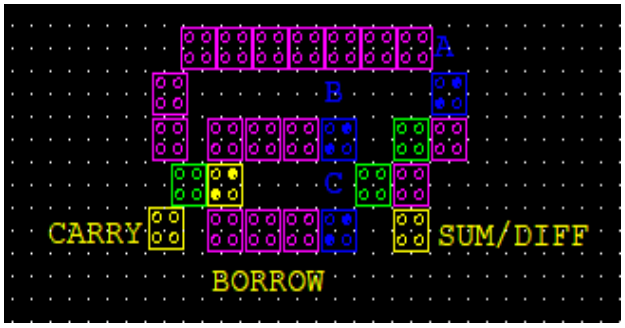


Fig 8: Block diagram of an adder-subtractor circuit

Inputs			Outputs			
A	B	C	Sum	Carry	Difference	Borrow
0	0	0	0	0	0	0
0	0	1	1	0	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	1	0	0	1	0	0
1	1	1	1	1	1	1

Table 3: Truth table of the adder-subtractor circuit

From the above truth table, it is clear that the Sum bit and difference bit is the same.The below figure shows the proposed design of the adder-subtractor circuit using the QCA designer tool.



(a)

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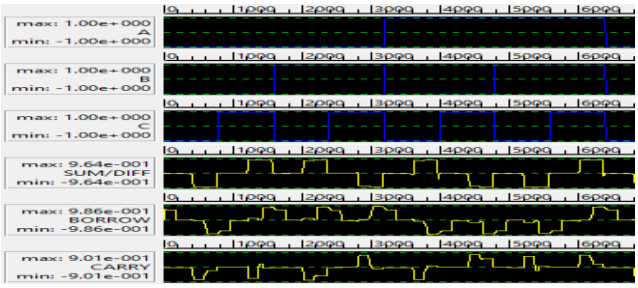

(b)

Fig 9:(a)adder-subtractor circuit in QCA, (b) its simulation result.

On counting the cells of adder-subtractor proposed here we can clearly see that our full adder design includes total 26 cells.

For calculating area we have to follow following steps which is shown below:

Step1: Here we can see total 9 cells are presented horizontally and each cell is having 18nm length and 18nm breadth so $18*18nm^2$ area is being occupied by each cell. So for 9 cells with the particular gap between cells 2nm and the gap between one cell from its last boundary are 1nm.

So the entire horizontal area of 9 cells = (1+18+2+18+2+18+2+18+2+18+2+18+2+18+2+18+2+18+1) = 180nm

Step2: Next we have on total 5 cells are presented vertically so by following previous similar calculation we have.

the entire vertical area of 5 cells = (1+18+2+18+2+18+2+18+2+18+1) = 100nm

step 3: Total area occupied = 180nm * 100nm = $18000nm^2$

So the area occupied by proposed design of full adder is about 0.018 μm^2.

IV.RESULT ANALYSIS

All previous research conducted in designing QCA circuits for adder-subtractor are compared and the table of comparison is shown in the figure below.

Comparison table of QCA Full adder-subtractor circuit

S.NO.	REFERENCE	CELL COUNT	AREA
1	REF[1]	228	0.400
2	REF[2]	186	0.132
3	REF[3]	180	0.190
4	REF[4]	109	0.790
5	REF[5]	90	0.110
6	REF[6]	83	0.090
7	REF[7]	75	0.090
8	REF[8]	54	0.060
9	REF[9]	53	0.039
10	REF[8]	38	0.030
11	**PROPOSED DESIGN**	26	0.018

Table 3: Comparision table of QCA Full adder- subtractor circuit.

The proposed QCA adder-subtractor circuit are designed and simulated successfully using QCA designer tool. From above comparison table we can see clearly that the design presented in this paper requires less cell count and due to a decrease in cells it also shows reduction in area. And thus found a better design for application.

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V. CONCLUSION

The design of a adder-subtractor QCA circuit is presented in this paper. The simulation result is tested in QCA Designer 2.0.3 tool and shows the correctness of the proposed circuit. After comparing the proposed design with all previous designs, the conclusion can be made that the proposed design gives satisfying result. In the future, we will work more to explore the new concept and then apply it to construct a more efficient adder-subtractor circuit in the QCA platform.

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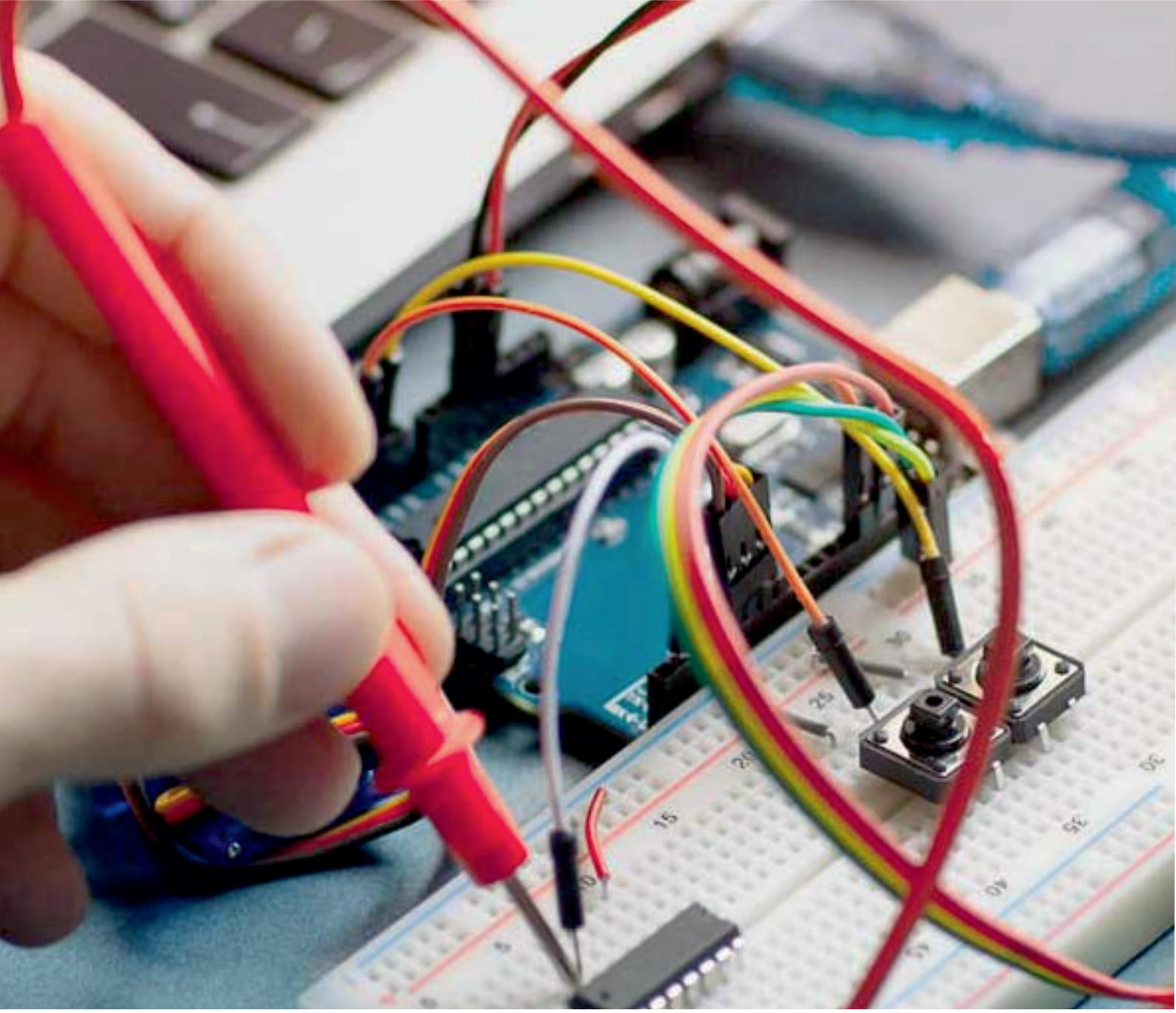

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